Program: TE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester V

Course Code: ETC403 and Course Name: Microprocessor & peripherals

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

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| Q1.  | In 8085, 16-bit address bus, which can address upto |
| Option A: | 16KB |
| Option B: | 32KB |
| Option C: | 64KB |
| Option D:  | 128KB |
|  |  |
| Q2. | There are \_\_\_\_\_\_\_ general purpose registers in 8085 processor |
| Option A: | 5 |
| Option B: | 6 |
| Option C: | 7 |
| Option D: | 8 |
|  |  |
| Q3. | This signal indicates that another master is requesting the use of the address and data buses. |
| Option A: | READY |
| Option B: | HOLD |
| Option C: | HLDA |
| Option D: | INTA |
|  |  |
| Q4. | Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0 |
| Option A: | Binary bit |
| Option B: | Zero flag |
| Option C: | Sign flag |
| Option D: | Overflow flag |
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| Q5. | MVI K, 20F is an example of |
| Option A: | Immediate addressing mode |
| Option B: | Register addressing mode |
| Option C: | Direct addressing mode |
| Option D:  | Indirect addressing mode |
|  |  |
| Q6. | The different ways in which a source operand is denoted in an instruction is known as |
| Option A: | Instruction Set |
| Option B: | Interrupts |
| Option C: | 8086 Configuration |
| Option D:  | Addressing Modes |
|  |  |
| Q7.  | Which of the following is not a data copy/transfer instruction |
| Option A: | MOV |
| Option B: | PUSH |
| Option C: | DAC |
| Option D:  | POP |
|  |  |
| Q8.  | Which of the following instruction is not valid. |
| Option A: | MOV AX, BX |
| Option B: | MOV DS, 5000H |
| Option C: | MOV AX, 5000H |
| Option D:  | PUSH AX |
|  |  |
| Q9. | In PUSH instruction, after each execution of the instruction, the stack pointer is |
| Option A: | incremented by 1 |
| Option B: | decremented by 1 |
| Option C: | incremented by 2 |
| Option D:  | decremented by 2 |
|  |  |
| Q10.  | The instruction that pushes the contents of the specified register/memory location on to the stack is |
| Option A: | PUSHF |
| Option B: | PUSH |
| Option C: | POPF |
| Option D:  | POP |
|  |  |
| Q11.  | The instructions that are used for reading an input port and writing an output port respectively are |
| Option A: | MOV, XCHG |
| Option B: | MOV, IN |
| Option C: | IN,MOV |
| Option D:  | IN,OUT |
|  |  |
| Q12.  | The instruction that adds immediate data/contents of memory location specified in an instruction/register to the contents of another register/memory location is |
| Option A: | SUB |
| Option B: | ADD |
| Option C: | MUL |
| Option D: | DIV |
|  |  |
| Q13. | Which of the following are known as Higher Address Bus? |
| Option A: | A15 - A8 |
| Option B: | AD7 - AD0 |
| Option C: | READY |
| Option D:  | WR |
|  |  |
| Q14.  | DMA stands for |
| Option A: | Display Memory Access |
| Option B: | Directly Memory Access |
| Option C: | Device Memory Access |
| Option D:  | Direct Memory Access |
|  |  |
| Q15. | How many types of Interfacing in 8086 |
| Option A: | 2 |
| Option B: | 3 |
| Option C: | 4 |
| Option D:  | 5 |
|  |  |
| Q16.  | In which type of communication, the interface gets a single byte of data from the microprocessor and sends it bit by bit to the other system serially and vice-a-versa |
| Option A: | Parallel Communication Interface |
| Option B: | Serial Communication Interface |
| Option C: | Both A and B |
| Option D:  | None of the above |
|  |  |
| Q17. | In 8086 microprocessor , the address bus is bit wide |
| Option A: | 12 |
| Option B: | 10 |
| Option C: | 16 |
| Option D: | 20 |
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| Q18. | Which pin/signal of ADC AD571 interfacing apprises about the accomplishment of data reading in the microcontroller so as to indicate ADC to get ready for the next data sample |
| Option A: | BLANK /CONVERT (high) |
| Option B: | BLANK/DR (low) |
| Option C: | DATA READY (DR) |
| Option D:  | All of the above |
|  |  |
| Q19.  | When the 82C55 is reset, its I/O ports are all initializes as |
| Option A: | output port using mode 0 |
| Option B: | Input port using mode 1 |
| Option C: | output port using mode 1 |
| Option D:  | Input port using mode 0 |
|  |  |
| Q20. | Which provide a mechanism to establish a link between the microprocessor and i/o device |
| Option A: | Input interface  |
| Option B: | Output interface  |
| Option C: | Both a and b |
| Option D: | None of these |
|  |  |
| Q21. | The processor of knowing the status of device and transferring the data with matching speeds is called |
| Option A: | Handshaking  |
| Option B: | Peripheral  |
| Option C: | Ports |
| Option D:  | None of these |
|  |  |
| Q22.  | The ADC is treated as an\_\_\_\_\_\_\_\_ device by the microprocessor. |
| Option A: | Input  |
| Option B: | Output |
| Option C: | Input/Output |
| Option D:  |  None of the above |
|  |  |
| Q23. | Which of the following are Features of 8255A |
| Option A: | It consists of 3 8-bit IO ports i.e. PA, PB, and PC. |
| Option B: | Address/data bus must be externally demultiplexed. |
| Option C: | It is TTL compatible. |
| Option D:  | All of the above |
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| Q24.  | It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus |
| Option A: | Read/Write Logic |
| Option B: | Data Bus Buffer |
| Option C: | system data bus |
| Option D:  | System Buffer |
|  |  |
| Q25. | Which of the following is not true features of 8257 |
| Option A: | It has three channels which can be used over three I/O devices. |
| Option B: | Each channel has 16-bit address and 14-bit counter. |
| Option C: | Each channel can transfer data up to 64kb. |
| Option D:  | Each channel can be programmed independently. |